REMARKS

Claims 1-23 are pending in the present application. Claims 1-23 have been rejected. Clams 1 and 19 are the only independent claims.

Rejections based on Yu et al.

Claims 1-6, 16, and 19 are rejected under 35 U.S.C. 103(a) as allegedly rendered unpatentable based on Yu et al. (U.S. Patent No. 6,180,543) alone. See point 2 of the Official Action.

In purportedly setting forth the *prima facie* case, the Official Action relies upon the limited disclosure in Yu at col.5, ll.10-20:

> Referring now specifically to FIG. **4**, there is shown a cross section of a semiconductor surface **10** after a nitride-oxide anneal of the substrate surface. The NO or N_2O anneal of the substrate surface is performed under a temperature of between about 600 and 800 degrees C. for a time between about 20 and 40 seconds (used to activate the dopants) and at a pressure below about 10^{-6} Torr. This anneal is a pre-oxidation anneal, which creates a layer **18** of nitrided oxide over the surface of the underlying substrate **10**. Layer **18** is a layer of oxide with a heavy concentration of nitride, this concentration of nitride has as yet no definitive concentration profile.

Applicants point out that neither in the above excerpt, nor anywhere throughout Yu et al. is there any teaching or suggestion that a chemical vapor deposition process or furnace be utilized as required by the claimed invention. Chemical vapor deposition is required in both independent Claims 1 and 19. The chemical vapor deposition aspect of Applicants' invention presents an improvement in the art that has not heretofore been appreciated or practiced based on the particular difficulties associated with nitriding an oxide layer in a method of forming a gated oxide. In addition, any teaching of a chemical vapor deposition process or utilization of a chemical vapor deposition furnace is completely absent from the teaching of Yu et al. Applicants' claimed method calls for this as a required element before any *prima facie* case can

be made out. As such, Applicants' claimed methods are both novel and non-obvious.

In addition, the pressure at which the NO or N_2O annealing is done in Yu et al. is at a mere 10^{-6} Torr. Although this type of pressure might be useful for doping in small quantities on the surface of a substrate as is practiced in Yu et al., it is not practical for deposition in a substantial amount as will occur in a chemical vapor deposition furnace according to Applicants' invention. Accordingly, Yu et al. does not teach or suggest the elements of the claimed invention and the *prima facie* rejection cannot be maintained.

Furthermore, with respect to Claim 2, there is no teaching or suggestion of a method wherein the oxide forming and nitriding steps are performed at approximately the same temperature. The formation of oxide and nitriding at approximately the same temperature is also a clear improvement to known processes and it is not in any way taught or suggested by Yu et al. In fact, there is no teaching or suggestion in Yu et al. of any temperature of a distinct oxidation step, as opposed to a nitriding step. With respect to Claim 3, there is no teaching or suggestion in Yu et al. of a method wherein the oxide forming step is performed at a pressure of about 1.5 atm. or less. With respect to Claims 4 and 5, there is no teaching or suggestion in Yu et al. of a method wherein the nitride forming step is performed at a pressure near 1.5 atm. or 1.0 atm., respectively. Finally with respect to Claim 6, there is no recitation throughout Yu et al. of an oxide forming step at a temperature of 800 °C. or less, much less both oxide forming and nitriding steps performed at a temperature of about 800 °C or less.

It is respectfully submitted that the Official Action has failed to establish a *prima facie* rejection in obviousness that Yu et al. meets the claimed invention. Reconsideration and withdrawal of the rejection of Claims 1-6, 16, and 19 is therefore respectfully requested.

Claims 7, 8, 17, 20, and 22 are rejected under 35 U.S.C. 103(a) as allegedly rendered unpatentable based on Yu et al. combined with Van Zant, "Microchip Fabrication, A Practical

Guide to Semiconductor Processing" (2000) 4th Ed., McGraw Hill, pgs. 156, 160, 188, 189, 503, 513, and 514. See point 3 of the Official Action.

The motivational statement in the rejection states: "Therefore, it would have been obvious to one of ordinary skill in the art to construct a ONO layer in a MOSFET structure." See sentence bridging pages 3 and 4. Applicants respectfully point out that the claimed invention is directed to a method of making while this rejection appears to be structured against a product claim. In addition, neither Yu et al. or Van Zant disclose a chemical vapor deposition furnace or process involving such a furnace. Clearly, Van Zant fails to cure the deficiencies of Yu et al.

In addition, neither Yu et al. or Van Zant teach or suggest a step of reoxidizing a semiconductor substrate in a second oxidation step after a nitriding step, a step of depositing a gate electrode layer on top of a nitrided oxide layer, a method wherein the oxide layer prepared is a dry oxide layer, a step of oxidizing a nitrided gate oxide layer on a substrate, or a step of depositing a gate electrode layer on top of a nitrided gate oxide layer on a substrate. Clearly, this combination of references fail to support a *prima facie* rejection of Claims 7, 8, 17, 20 or 22.

For the reasons set forth above, Yu et al fails to teach or suggest the elements of Claims 7, 8, 17, 20, and 22. Van Zant does not cure the deficiencies in Yu et al. as Van Zant is cited merely to illustrate that oxide/nitride sandwiches are known in semiconductors. Neither Yu et al. or Van Zant provide any motivation to combine the disclosures for this reason. Van Zant also fails to cure the deficiencies in Yu et al. as Van Zant contains no teaching or suggestion, nor provides any motivation to include a chemical vapor deposition process or furnace with the disclosure in Yu et al.

The following rejections are treated together as the issues coincide, and for many of the same reasons as treated above.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as allegedly rendered unpatentable

based on Yu et al. combined with Van Zant and Tseng (U.S. Patent No. 5,766,994). See point 4 of the Official Action.

Claims 11, 12, and 23 are rejected under 35 U.S.C. 103(a) as allegedly rendered unpatentable based on Yu et al. combined with Van Zant and Tseng and the Specification. See point 5 of the Official Action.

Claims 13-15 are rejected under 35 U.S.C. 103(a) as allegedly rendered unpatentable based on Yu et al. combined with Van Zant and Kawakami (U.S. Patent No. 6,399,520). See point 6 of the Official Action.

Claims 18 and 21 are rejected under 35 U.S.C. 103(a) as allegedly rendered unpatentable based on Yu et al. combined with Van Zant. See point 7 of the Official Action.

As noted above, Van Zant fails to cure the deficiencies of Yu et al., which include, among other things, a failure to teach or suggest a chemical vapor deposition furnace. The remaining references also fail to cure this deficiency.

Tseng (U.S. Patent No. 5,766,994) is cited to purportedly demonstrate the formation of a tungsten silicide layer over top of a previously formed polysilicon layer. Tseng does not teach or suggest the use of chemical vapor deposition in any way throughout that disclosure. Kawakami et al. (U.S. Patent No. 6,399,520) is cited to purportedly demonstrate formation of a silicon oxide layer having a depth of 20 angstroms. However, Kawakami et al. relies upon the use of plasma deposition, and in fact, teaches way from the utilization of chemical vapor deposition in forming films having nitride stating "[w]hen SiN films are deposited by use of the CVD method, there occur many incomplete bonds (dangling bond) at the interface with the silicon substrate to result in deterioration of semiconductor property. Accordingly, in forming SiN films, it is considered very promising to directly nitride a silicon substrate using plasma." See col.1, ll.33-38.

Accordingly, neither Tseng or Kawkami et al. cure the deficiencies of Yu et al. and Van

Zant. It is respectfully submitted that the Official Action has failed to establish that the methods claimed are *prima facie* obvious. Reconsideration and withdrawal of all the rejections is respectfully requested.

CONCLUSION

All rejections having been addressed by the present amendments and response, Applicants submit that the present case is in condition for allowance and respectfully request early notice to that effect. If any issues remain to be addressed in this matter which might be resolved by discussion, the Examiner is respectfully requested to call Applicants' undersigned counsel at the number indicated below.

Respectfully submitted,

PIPER RUDNICK LLP

Steven B. Kelber
Registration No. 30,073
Attorney of Record

Patrick R. Delaney
Registration No. 45,338

1200 Nineteenth Street, N.W.
Washington, D.C. 20036-2412
Telephone No. (202) 861-3900
Facsimile No. (202) 223-2085

SERIAL NO. 09/975,256
DOCKET NO.: 8229-014-27

MARKED-UP COPY OF PARAGRAPHS, AS AMENDED

On page 6, at lines 8-17, please replace the paragraph there with the following paragraph as follows:

A conventional method for incorporating nitrogen into a gate oxide layer comprises annealing a preformed oxide layer in the presence of nitrous oxide gas (N_2O). Annealing with N_2O, however, is generally not effective in incorporating more than 1 to 1.5 [at. %] wt.% of N in the gate oxide layer. Additionally, in order to achieve significant nitrogen incorporation using N_2O gas, it has been found necessary to pre-heat the gas before it enters the furnace. Preheating is usually conducted by flowing the N_2O gas through a torch that is maintained at a temperature of from 800 °C to 950 °C. A helical torch is typically employed to increase the residence time of the gas in the torch. The N_2O nitridation anneal itself is typically conducted at temperatures in excess of 900 °C.

SERIAL NO. 09/975,256

DOCKET NO.: 8229-014-27

MARKED-UP COPY OF AMENDED CLAIMS

1. (Amended) A method of forming a gate oxide layer on a semiconductor substrate comprising:

forming an oxide layer on the substrate by oxidizing the substrate in a [CVD] chemical vapor deposition furnace;

introducing nitric oxide (NO) gas into the [CVD] chemical vapor deposition furnace; and

nitriding the oxide layer in the presence of the nitric oxide gas.

16. (Amended) The method of Claim 1, wherein at least 1.5 [at.%] wt.% of N is incorporated into the oxide layer during the nitriding step.

19. (Amended) A method of nitriding a gate oxide layer on a semiconductor substrate comprising:

nitriding the gate oxide layer in the presence of nitric oxide (NO) gas;

wherein the nitriding step is conducted at a temperature of about 800°C or less and at a pressure of about 1 atm or less in a chemical vapor deposition furnace.